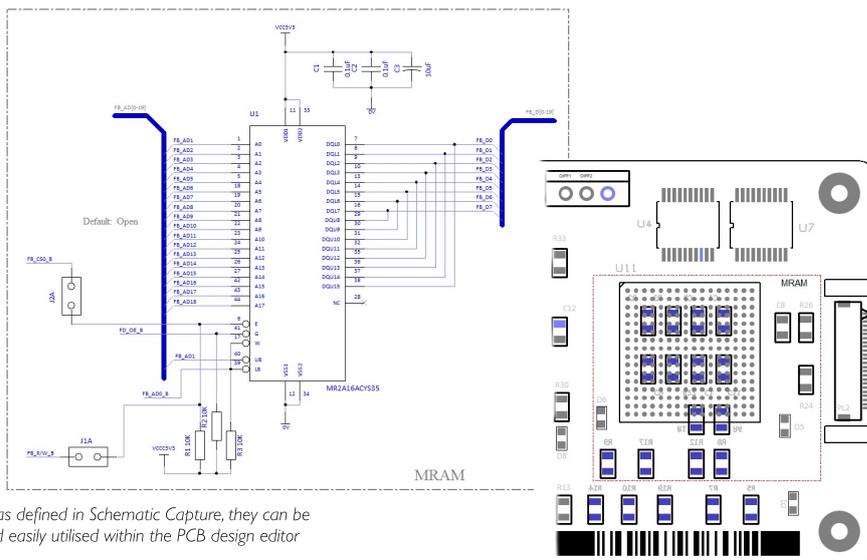


# Pulsonix Version 10.5 Update

## Define Constraint Areas in Schematic Editor

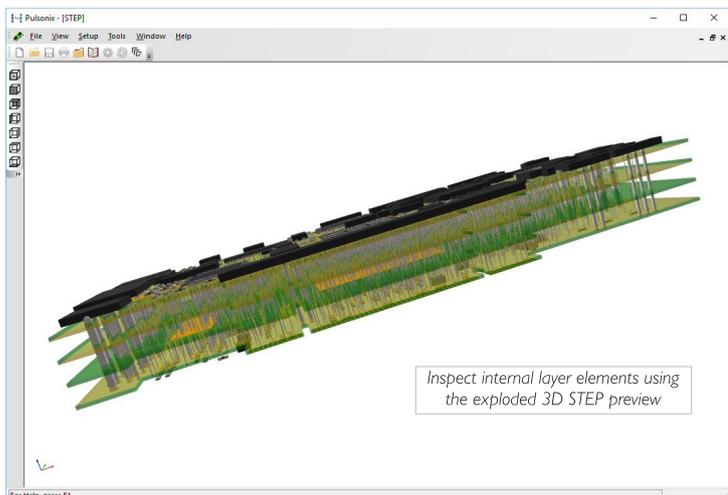
Within the Schematic Capture editor, you can now add Areas. These behave as active regions that can be used in the constraint manager to define rules without the need to assign rules to individual items, making rules allocation much faster. Rules can be Net or Component based and subsequently passed through into the PCB design environment. The rules definition is brought much further forward in the whole design process. With areas defined in the Schematic, they can also be used as plotting zones to control plot outputs.



With Areas defined in Schematic Capture, they can be fully and easily utilised within the PCB design editor

## STEP 3D Preview

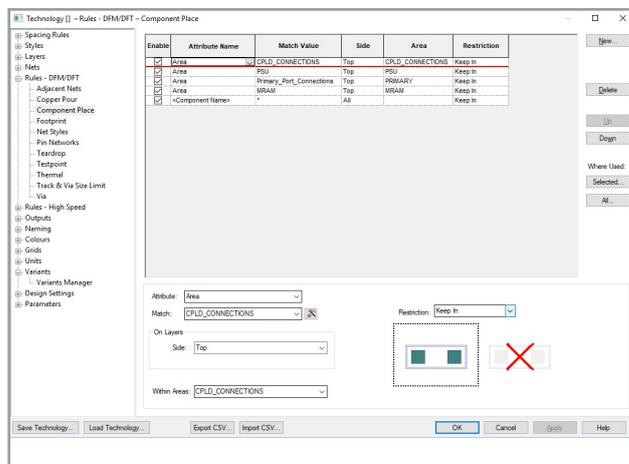
Significant enhancements in the 3D STEP Preview improve the flow between the Pulsonix PCB and 3D codesign environments. The ability to save enclosure positional changes between 3D and PCB has been added so that exact positioning can be achieved. An exploded view provides users with a view 'inside' the PCB layer structure allowing them to inspect copper and vias internally. Clash markers show the precise location of rules violations and the rule in error. A measure tool enables distances between objects in the 3D Preview to be viewed. Visualisation is improved with a Board Transparency option and user defined spotlight position.



Inspect internal layer elements using the exploded 3D STEP preview

## Component Place Rules in PCB

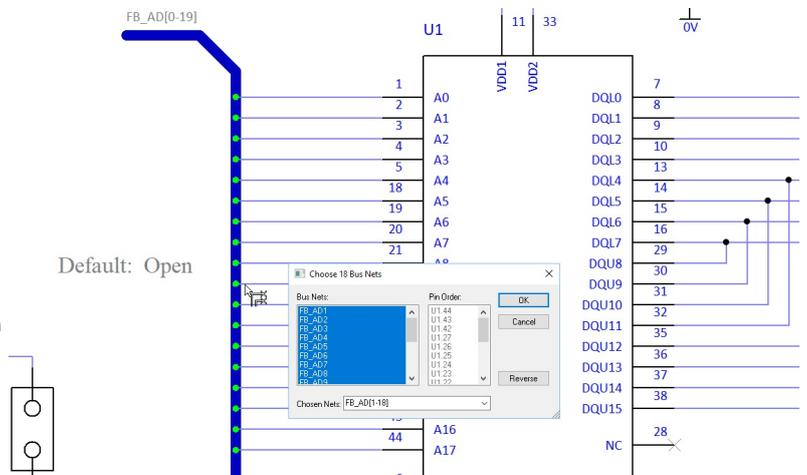
Component Placement rules can be defined using Areas and Attributes. With Areas defined in the Schematic design and Components then assigned to them, the place rules can be used. Defining collections of critical Components means localised areas in PCB are utilised by the Pulsonix placement tools and rules.



The powerful rules mechanism enables Component Placement to be pre-defined for use in the PCB design editor

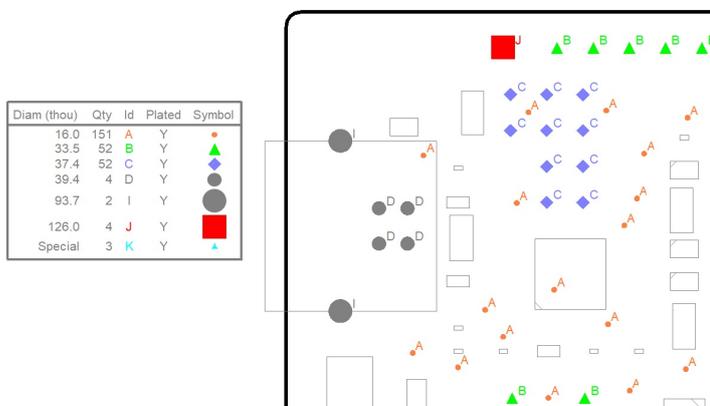
## Multi Connect in Schematic Designs

A new feature within V10.5 enables users to multiselect pins within the Schematic design, and to draw these connections as a set of 'bused' nets. Functions are provided to pull these sets of nets together at the same time so that drawing many connections saves precious design time. As well as Bused Net, the ability Auto Weld a symbol to a bus has been added. By touching the pins of a symbol on the bus, weld markers indicate it can be connected. Moving away will then make the connection structure and display the Net Names allocated from the bus. All bus rules are adhered to; terminal directions and net name positions.



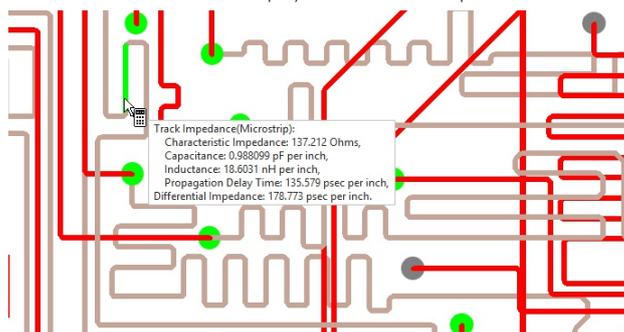
## Drill Drawing Layers

Drill drawing layers can now be included in PCB along with the drill ident. This adds further documentation detail to the design and complements the existing plotting mechanism for drill drawings. Where drill idents are required on other layers, these can be allocated using a Drill ID attribute position. In addition, coloured Drill Sizes can be used to define drill idents by colour for further clarity and identification.



## Dynamic Track Impedance Calculation

Track Impedance calculations can be displayed on the fly using the Design Calculator tool in 'dynamic' mode. All calculations are shown in real time for a selected track with the results displayed in the head-up display tooltip.



## Feature Summary:

- Merge Styles in Technology
- Square Ended Thermal Spokes
- Block Instance – Edit Symbol in Place
- Regenerate Block Instance – Reset Pins
- Drag and Drop facility for Library Manager
- Design Colours loaded during Eagle Import
- DXF Output in Panel Editor
- Improved Tab routing rules for Panel Editor
- Graphics Declutter option
- Fill-in Gaps In Number Ranges
- Text Callouts with Solid Colour Background
- Export OrCAD Netlist Export – Suppress Net/Part Names
- Support for 3D Space Mouse in STEP 3D Preview
- Additional Star Point Items in PCB
- Set Pour Order a Modeless Dialog
- Ability to Enable/Disable Rules
- Ability to add Notes to a Rule
- Cell Notification of Rule Errors
- Filter Net Names column
- Suppress Unconnected Lands for Micro-Vias
- Lock Aspect Ratio and Scale for a Bitmap
- Export all output formats through Plotting dialog